



RISC-V Software Ecosystem

Rainer Leupers

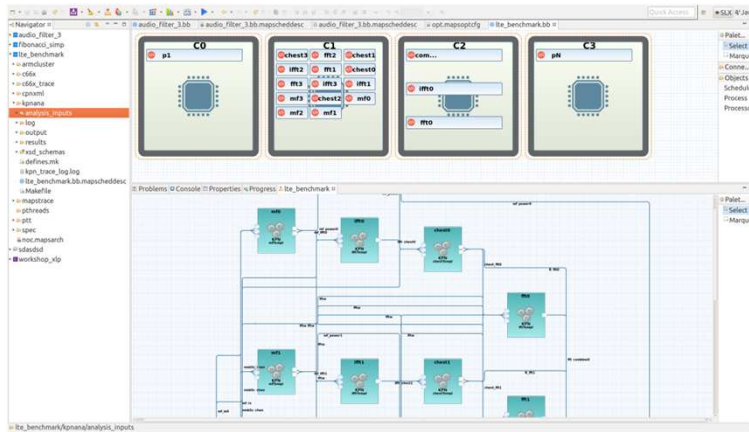


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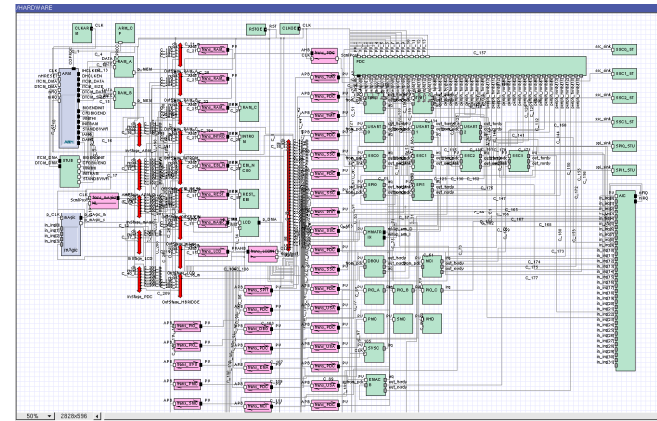


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Our R&D topics in HW/SW co-design technologies



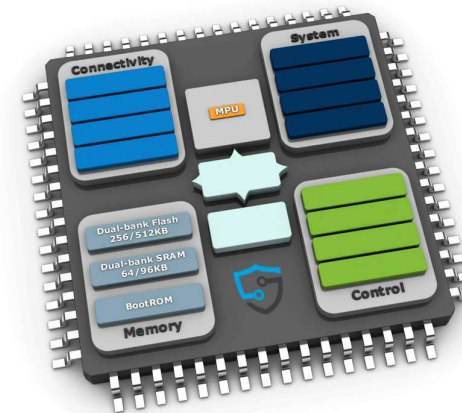
Embedded SW development tools



System-on-chip HW design



Virtual prototyping



Hardware security

Scientific and technological expertise

- Numerous **EU projects** in HW/SW codesign:
 - ARTIST, SHAPES, EURETILE, DSPACE, GEMSCLAIM, **HIPEAC**, **TETRACOM**, Eurolab4HPC, **TETRAMAX**, BOWI, EDIH Rheinland



- Academia-to-industry **tech transfer**:
 - Infineon, Synopsys, Ericsson, Microsoft, Tokyo Electron, ACE, Huawei, HiSilicon, Ricoh, Samsung, Audi/Cariad



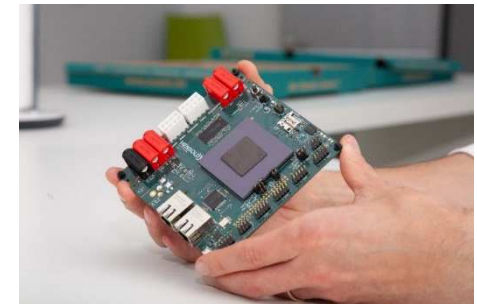
- Eight successful **spin-off companies**, e.g.
 - **LISATek**: founded 2002, acquired by CoWare/Synopsys
 - **Silexica**: founded 2014, acquired by Xilinx/AMD
 - **MachineWare**: founded 2022



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RISC-V instruction set architecture (ISA)

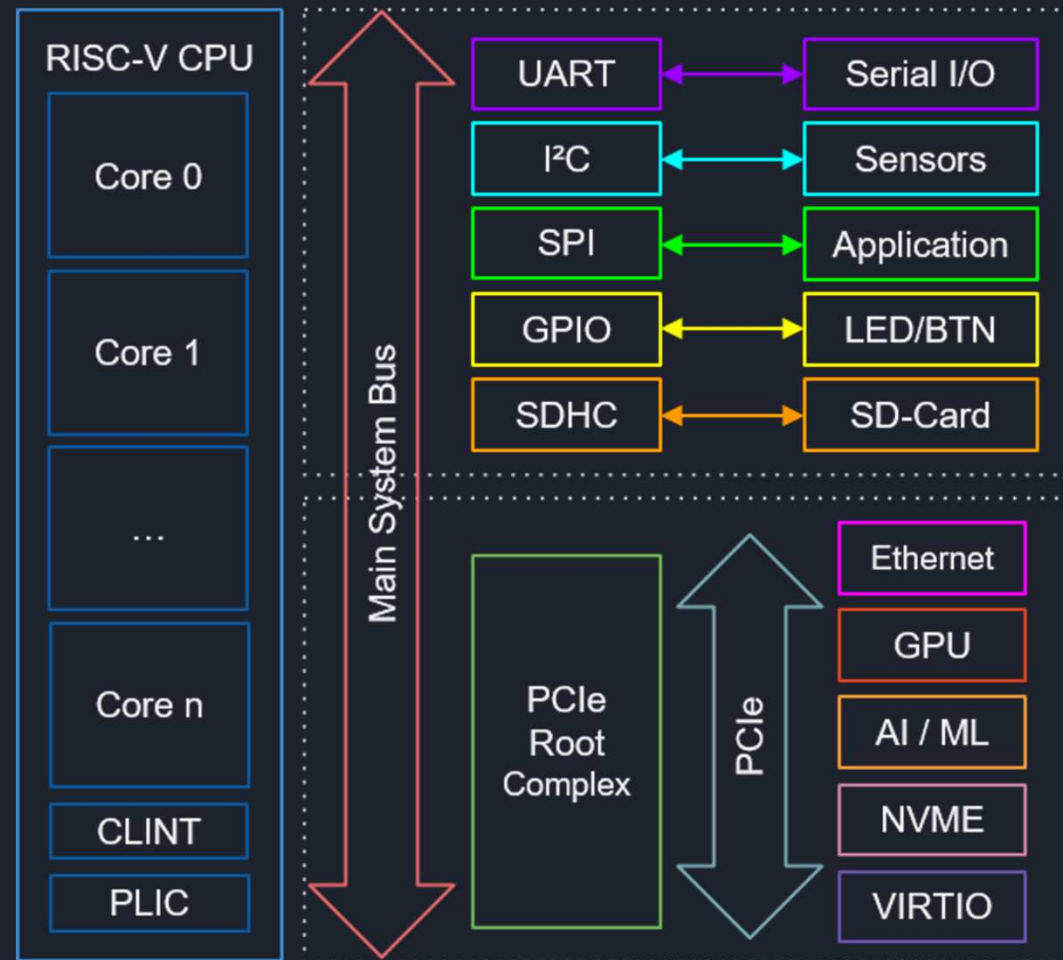
- Programmable **processor (CPU) architecture** developed at UC Berkeley in 2010
- **Open ISA standard** (not “open source”)
- First widely accepted open ISA, broad **academia and industry support**
- Available to anyone **w/o license costs**
- Easy to **scale** and to **customize**
- Major **challenges**:
 - Competitive landscape (e.g. ARM)
 - Identify application sweet spots and configurations
 - Develop **comprehensive SW and tools ecosystem**



MachineWare GmbH Products & Services

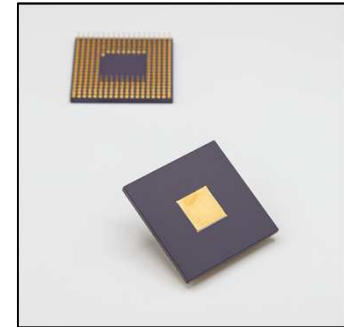


- Virtual Prototypes based on SystemC
- Fast CPU Instruction Set Simulators
 - SIM-V (RISC-V ISS)
 - SIM-A (ARM ISS)
- Qbox/QEMU
- ARM-on-ARM
- Services
 - SystemC, QEMU Modeling
 - Training & Consulting



Desired EU partnerships related to RISC-V

- Major application domains:
 - automotive, telecom, AI, critical infrastructures
- Use of **Virtual Prototypes** for
 - SW development and verification
 - System-on-chip design
 - CPU customization
 - Cybersecurity
- **Contact info:**
 - Prof. Dr. Rainer Leupers
 - leupers@ice.rwth-aachen.de
 - www.ice.rwth-aachen.de
 - <https://www.linkedin.com/in/rainer-leupers-135b344>
 - www.machineware.de
 - <https://www.linkedin.com/company/machineware>



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